# Intelligent Methods for Test and Reliability

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***Abstract*—Test methods that can keep up with the ongoing increase in complexity of semiconductor products and their underlying technologies are an essential prerequisite for maintaining quality and safety of our daily lives and for continued success of our economies and societies. There is a huge potential how test methods can benefit from recent breakthroughs in domains such as artificial intelligence, data analytics, virtual/augmented reality, and security. The Graduate School on "Intelligent Methods for Semiconductor Test and Reliability" (GS-IMTR) at the University of Stuttgart is a large-scale, radically interdisciplinary effort to address the scientific-technological challenges in this domain. It is funded by Advantest, one of the world leaders in automatic test equipment. In this paper, we describe the overall philosophy of the Graduate School and the specific scientific questions targeted by its ten projects.**

## I. Introduction

Semiconductor technology has been a foundation of scientific progress, societal development and economic growth since decades. Test methods are a main pillar of this technology and are an essential prerequisite for obtaining high-quality products, from low-cost consumer segment to enormously complex and safety-critical installations, at reasonable cost. As a scientific area, test methods are currently undergoing a transformation triggered by the advent of next-generation artificial intelligence technology. Therefore, a new, radically interdisciplinary and large-scale research effort is needed to enable the products of tomorrow and meet the needs of their makers.

To give a major impetus on applied semiconductor test and reliability research, Advantest and the University of Stuttgart jointly established a Graduate School on "Intelligent Methods for Semiconductor Test and Reliability" (GS-IMTR). Advantest, a major automatic test equipment (ATE) vendor, has first-hand understanding of the technological developments pursued by its customers and their practical needs; it also has access to relevant technology data. GS-IMTR directly supports ten PhD candidates in projects selected using a competitive peer-review-based process; one Assistant Professor (Juniorprofessor in German); and the required infrastructure for six years. These projects are stemming from a broad set of partner institutes that bring in interdisciplinary expertise in fields as diverse as machine learning; visualization; security; radio-frequency circuit design; emerging technologies and architectures. The last of the ten projects has started in the beginning of 2021, and therefore the Graduate School is still in an early phase.

GS-IMTR supports international exchange by inviting academic and industrial researchers from abroad and providing the funded PhD candidates with opportunities for stays abroad. In addition, GS-IMTR can associate further PhD candidates from the University, who are funded from other sources but work on related topics, thus forming a strong University-wide nucleus on test research. The Graduate School includes an Advisory Board consisting of international researchers, representatives of Advantest, and professors of the University. It determines the strategic research orientation of the school, organizes peer-review of PhD project proposals, makes funding decisions, and oversees the progress of the projects.

The need for a heavily interdisciplinary and data-driven approach is underscored by Fig. 1, which presents a detailed view of today's test processes being placed between design, fabrication and in-field operation of integrated circuits. Test usually consists of several *test insertions*, each with its own requirements. In general, different assembly and test (OSAT) providers are in charge of the individual test insertions. In addition, post-silicon validation (PSV) and characterization are run before the start of volume fabrication, creating non-trivial interactions between the (fabless) design house and the fab (foundry). Test-related data collected during all these steps contains valuable information, which is heavily under-utilized today. To this end, GS-IMTR brings together specialists on test and reliability with researchers working on a broad range of interdisciplinary topics.

The remainder of this paper introduces the research questions investigated by GS-IMTR's ten peer-reviewed projects P1 ... P10 and by (currently three) associated projects PA1 ... PA3. Fig. 1 provides a rough positioning of all projects within the test value chain. Note that the numbering of the projects is based on the time of their acceptance rather than on their thematic coherence; therefore we organize the following content by larger topic areas to which the individual projects belong.

## II. Intelligent Methods for PSV and Beyond

The first three projects discussed in this section focus on post-silicon validation. They provide machine-learning methods for tuning parameters, for selecting most relevant variables, and visually explaining to engineers the issues identified during PSV. The fourth project applies brain-inspired Hyperdimensional Computing to chip testing towards improving the yield.

### A. Self-Learning Tuning for Post-Silicon Validation (P3)

In PSV, devices under test (DUTs) are examined to identify tuning parameters such that the DUTs meet their specifications

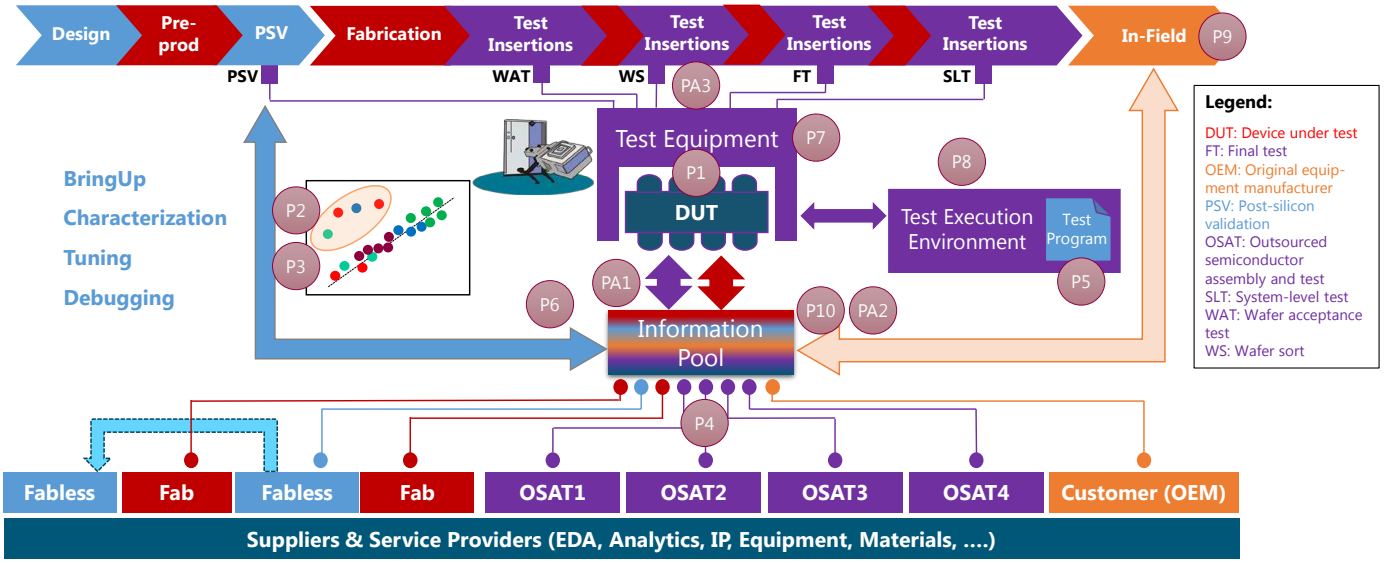


Fig. 1. Test-oriented circuit design and manufactured flow with GS-IMTR's projects.[1]

under all operating conditions. This project aims to determine a tuning law or sweet spots for tuning based on randomly generated test data from one or multiple DUTs. The goal is to develop a generic, data-driven approach that automatizes the PSV tuning task, copes with less assumptions, and scales well. We deal with up to a few hundred conditions and tuning parameters as input and several output parameters. Depending on the context, one refers to parameters, variables, or dimensions.

Conventionally, the identification of tuning configurations relies on classical point-wise optimization methods. Point-wise optimization methods such as Powell's method [1] assume certain properties of the objective function or approximate the objective to fulfill these properties. Given the properties, the methods implement different iterative strategies to converge to the optimal tuning configuration. This approach is insufficient and makes it difficult to allow more flexibility and robustness with respect to function properties. An approach based on random search is also impractical due to the high-dimensional parameter space and the related curse of dimensionality. However, flexibility and robustness are essential in PSV because the properties of the objective function are unknown even for experts. Due to process variations in the manufacturing process, devices are black-box functions with varying performances. In case of severe problems in manufacturing, devices can even be faulty. Moreover, classical point-wise methods are not well suited to optimize mixed data types in high-dimensional parameter spaces and thus often perform poorly in such setups.

As DUTs have very unique properties including heterogeneous parameters (numerical, integer, nominal) and non-smooth dependencies, the aim is to learn a tuning law in an adaptive, self-learning way. Therefore, we aim to follow the path of *learn-to-optimize* and examine approaches based on *reinforcement learning* for deep neural networks, *active learning*, and novel approaches to optimization as seen in [2].

The resulting methodology will lead to a deployable tuning law that is robust and flexible. The project is closely related to the projects P6 and P2. P2 will use the results and the gathered knowledge about the input-output relationships to visualize and possibly guide tuning as well as test case generation in interaction with human experts. P6 will benefit from robust solutions that detect or compensate influences of faulty devices (e.g. [3]) to employ deep learning (DL) variable selection methods based on test data, while this project can benefit from information about learned sets of input variables.

### *B. Deep Learning Based Variable Selection for Post-silicon Validation (P6)*

As mentioned before, DUT in modern PSV is often equipped with tuning knobs with up to hundreds of process parameters. To enable an efficient tuning and debugging of DUT by human experts, a few most important variables must be identified for visualization (e.g. P2) and efficient modeling (e.g. P3). This has been typically done based on expert knowledge and conventional statistical approaches. They are, however, not scalable to high-dimensional data. This project aims to leverage DL techniques for variable selection with high scalability for PSV.

In order to achieve this goal, we have proposed a novel feature mask (FM) module [4, 5] that can be jointly trained with a neural network for solving a regression task to predict a given target variable. After that, the FM module generates an importance vector, each element of which indicates the importance of the corresponding candidate variable. Specifically, the FM module has only linear complexity w.r.t. the data dimension, while most conventional methods have exponential complexity. This property ensures an efficient selection even for a large number of input variables. Furthermore, the FM method does not introduce sensitive hyperparameters so that even non-DL-experts can use it without difficulties. Last but not least, the implementation is highly modular and the FM method can be easily integrated into existing PSV tools. As future research, we plan to explore more use cases of the FM method in the entire semiconductor industry, including but not limited to test selection and measurements reduction.

[1]Image Source: https://www.gs-imtr.uni-stuttgart.de

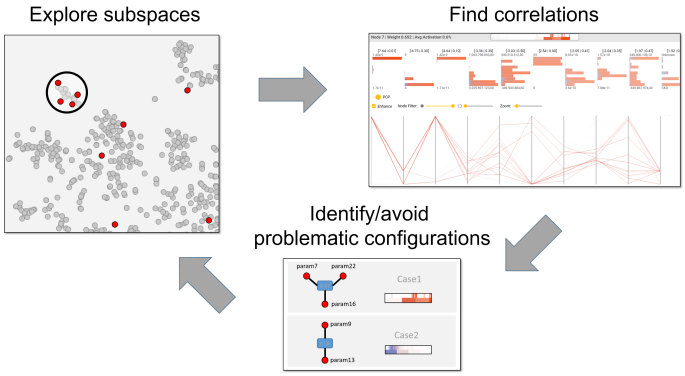


Fig. 2. Abstraction of the proposed visual analytics process

### C. Visual Analytics for Post-Silicon Validation (P2)

Visual analytics is a subfield of visualization research that tightly incorporates automatic methods and interactive visualization techniques into coherent approaches. Visual analytics approaches are in particular suitable for situations where applying fully automatic solutions is impossible due to problem complexity and where manual analysis is inappropriate because of data size and dimensionality [6, 7]. Our project aims to tackle some of the ill-posed challenges occurring in post-silicon validation and chip tuning with visual analytics methods, to speed up problem analysis while making it more reliable and accountable. For this purpose, we develop interactive workflows, shown in Fig. 2, that integrate validation engineers into human-computer analysis loops. By visually explaining the problems detected during post-silicon validation to engineers, we help them steer subsequent analysis methods to test hypotheses, to drill down into problems, or to find good chip settings avoiding issues. The result of such analyses is again visualized for further interactive refinement and exploration, closing the analysis loop.

To support engineers in understanding chip validation data and the problems it contains, we develop different visual representations to show large numbers of high-dimensional validation results in a digestible form. This comprises scatterplots that are generated through dimensionality reduction techniques (e.g., t-SNE [8] or UMAP [9]) as well as other solutions capable of depicting multi-dimensional data in a comprehensible manner including matrix-based views, customized node-link representations with glyphs, and parallel coordinates plots [10]. In addition, we aim to visually explain multivariate correlations of input value ranges and out-of-spec behavior as well as sensitivity of the validation data. From these visual representations of validation data, users can select subsets for further processing or detailed visualization and inspection.

The methods to analyze subsets of interest include machine learning techniques for both traditional approaches, but also more recent neural network-based ones that generate results, which can be visually explained in an accountable way and fast enough to be integrated into an interactive approach [11]. The models created from such local analyses can then be used to further restrict or broaden filter criteria for the data sets under inspection to understand which inputs cause which problems.

### D. Hyperdimensional Computing for Chip Testing—Towards Learning Fast from Little Data (P10)

This project explores for the first time how principles from brain-inspired Hyperdimensional Computing (HDC) can be applied to chip testing towards improving the yield [12]. The promises of HDC are: 1) strong robustness against noise and randomness in data, 2) ability to perform fast learning, and 3) ability to learn from little data. These aforementioned properties of HDC make it a very promising method for chip testing when it comes to advanced sub-5nm technology nodes because at such extreme scales, new emerging problems start to challenge the existing learning methods (e.g., deep neural networks and other traditional machine learning methods). These challenges can be summarized as follows:
1) The very noisy measurements due the inherent randomness caused by quantum mechanisms which become dominant at the 5nm technology node and below. Hence, the robustness of the learning method against noise becomes essential. 2) The necessity of an intelligent method to *selectively collect* the data measurements because the accuracy of deep learning methods heavily depends of the quality of input data. Hence, performing very fast learning during the measurement phase itself (i.e., during data collection) to enable *active leaning* become increasingly important. 3) The overwhelming complexity of circuits and systems in sub-7nm technology leads to more seldom problems in which the availability of data to *learn* those seldom problems is extremely limited. Hence, learning from little data becomes a key.

## III. Test Application

The three projects in this section consider test applications from rather different points of view. P7 designs an extension to ATE for applying radio-frequency (RF) test signals, covering the frequency ranges of several important emerging applications. P8 deals with optimizing software used for test application and ensuring its quality. P4 aims at achieving secure processing of sensitive manufacturing-related data on an ATE while keeping their confidentiality, by using modern secure multi-party computation protocols.

### A. Miniaturized Millimeter-Wave RF Interface Module (P7)

This project addresses the research area “Advanced design methodologies for testing next generation and beyond RF devices” by proposing a miniaturized and multi-functional frequency extension into the high millimeter-wave frequency range for RF testing. One goal of this project is to cover the frequency range from 17 to 90 GHz to enable testing for applications such as 24 GHz ISM, i.e., from K-band to E-band, including important frequency ranges like 77 to 79 GHz for automotive radar or 81 to 86 GHz fixed wireless point-to-point links by using high-speed semiconductor technologies (see Fig. 3).

The transceiver module is designed to be coupled to a 20 GHz RF base card from Advantest. The project covers the most challenging components of an entire transceiver chain including RF up-conversion, RF multi-pole switching, RF adaptive power amplification, RF filtering and LO multiplication over the entire frequency range (see Fig. 4).

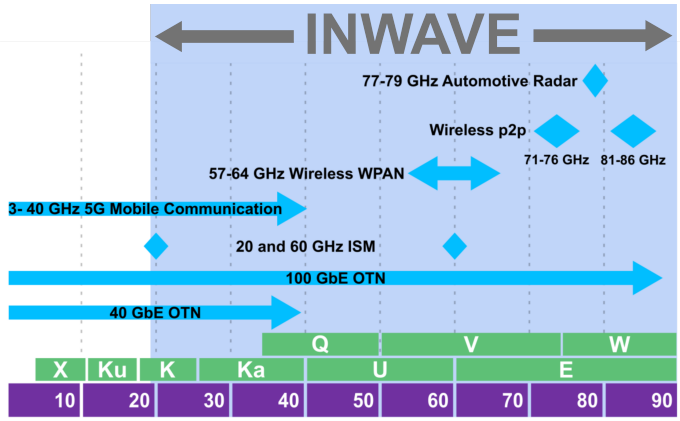


Fig. 3. Target Operational Frequency Range of the INWAVE transceiver module.

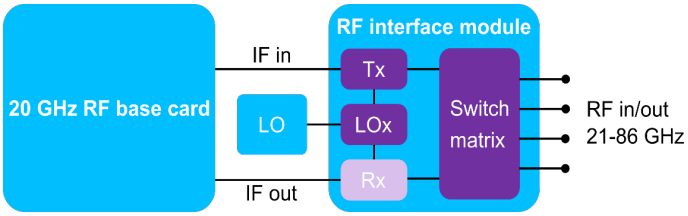


Fig. 4. Signal processing and transceiver chain.

For the implementation of the INWAVE interface module with its challenging requirements in terms of bandwidth (136 % relative RF bandwidth, 4 GHz IF bandwidth), dynamic range (>70 dB adjacent channel power ratio in a power range of −60 to +15 dB), and linearity (high OIP3), we consider two alternative approaches: a hybrid integration that will select the most suitable semiconductor technology for each element of the design, and a compact system on chip (SoC) version based on a state-of-the-art CMOS process (e.g., 22 nm FD-SOI).

### *B. Software Test Suite Optimization for Complex High Data-Volume Software (P8)*

Software plays a vital role in large-scale hardware testing. Test programs allow hardware testers to deal with the complexity of modern chips and enable them to automate the tests. A tester operating system and development environment (TOSDE) connects the customer test programs to the test system with the DUT. The TOSDE is a complex high data-volume software, for which it is extremely challenging to provide and assure the requested level of correctness, robustness, and performance. This is due to the ecosystem being many-fold and only partially under the control of the ATE platform developers. For instance, typical test system hardware handles millions of instructions per second running an embedded software that communicates with the tester operating system. Customers define and/or generate test programs. As a result of growing chip complexity, the test program complexity and the resulting data volumes are growing exponentially. Hence, this leads to performance-related questions about the TOSDE, including data transfer rates to local discs and network drives.

In this project, we develop and evaluate a novel approach to analyze and optimize software test suites for correctness, robustness, and performance. The particular focus is the support for testing high and exponentially growing data-volume software in a context in which unknown code (test programs) will run on top of this software, which has not been considered by previous approaches. We started by analyzing existing test suites. We found that mutation testing and a variant of it can be applied to identify untested code [13]. To extend the test suites, generating tests using fuzzing seems like a promising approach to tackle the vast space of possible test programs. Yet, to overcome the problems discussed above, we need to find a novel combination of tailored techniques from functional (e.g., coverage analysis, fuzzing, mutation testing) and non-functional testing (e.g., operational profile-based scalability testing), as well as model-based performance analysis (e.g., antipattern detection, what-if-analysis). This will allow us to decide what is interesting and important to test so that we get enough performance to handle the high data-volume while reducing the test execution time to feasible levels. We will evaluate all techniques in empirical analyses using an industry-leading TOSDE software and open-source systems.

### *C. Secure and Privacy-Preserving Semiconductor Testing (P4)*

Semiconductor testing plays an important role in the semiconductor manufacturing process. The tests not only ensure the quality of individual chips, but the data obtained during the tests is used to improve the manufacturing process itself. Manufacturers often use third-party services (shown as OSAT and service providers in Fig. 1) to perform the tests and evaluate the test data, as this requires special expertise. Since the test data and the models and methods to evaluate the data, such as machine learning models, are typically highly sensitive trade secrets, on the one hand, semiconductor manufacturers are reluctant to share their test data with third-party test services, and on the other hand, those services do not want to reveal information about their evaluation methods and models.

The idea of the project is to use, further develop and adapt a well-established cryptographic technique called secure multi-party computation (MPC) to protect the digital assets in a globalized and distributed semiconductor manufacturing flow. MPC allows two or more parties to evaluate a function on the local inputs of the parties without the parties revealing their inputs to the other parties. While MPC has been invented in the 1980s by Andrew Yao [14], MPC is currently a very active and hot research topic both in academia and industry since it is one way to solve the problem of privacy-preserving data processing.

However, in order for this approach to work, MPC has to be tailored to the specific requirements of the project. Whether or not these requirements can be met also depends on the type of test data and evaluation algorithm. At the end of the project, we would like to have a library that supports efficient privacy-preserving semiconductor testing for a big class of test data and evaluation algorithms, ideally with various levels of security. Test services should be able to easily and automatically compile their evaluation algorithms into MPC protocols that can then be carried out by them and the semiconductor manufacturers.

TABLE I
SLT ASPECTS CONSIDERED IN GS-IMTR RELATED TO TRADITIONAL TEST

| | **Traditional Test** | **System-Level Test** |
|---|---|---|
| Covered defects | Gross and marginal | Unknown → Project P1 |
| Coverage metrics | Fault coverage | Lacking → Project P5 |
| Test quality assessment | Fault simulation | Systematic technology lacking → Project P1 |
| Test generation | ATPG, manually written test programs | Reusing OS and application software → Project P5 |

## IV. TEST OF EMERGING TECHNOLOGIES AND SYSTEM PARADIGMS

The first two projects in this section focus on System-level test (SLT) [15, 16] (see Fig. 1), a test insertion based on workloads such as booting an operating system while the integrated circuit is mounted on a special board that includes memories and peripheral interfaces found in its target system. They investigate failures detected by SLT but not by prior test insertions, and targeted generation of suitable SLT workloads. Tab. I summarizes the essential research gaps closed by these projects. The final project focuses on the self-heating effects that manifests itself in advanced technology nodes, and its implications to test and reliability.

### *A. Systematic Analysis of System-level Test Fails (P1)*

The scientific objective of P1 is to establish a theoretical and systematic understanding of mechanisms behind *SLT-unique fails*, i.e., erroneous conditions that manifest themselves during SLT but not during conventional structural or functional test. The initial hypotheses for the origin of SLT-unique fails are: (1) complex defect mechanisms not covered by standard automatic test pattern generation (ATPG) tools; (2) systematic ATPG coverage holes (e.g., defects in clock trees); (3) effects of marginal defects during system-level interactions. To this end, an experimentation platform of sufficient complexity to reproduce these possible causes will be created within the project.

A further objective of Project P1 is to propose solutions to counteract SLT-unique fails. While complex defect mechanisms can be targeted by existing *cell-aware test* tools [17], special design-for-testability infrastructure can make SLT-unique fails detectable during regular test application. A better understanding of causes for SLT-unique fails can lead to design rules and guidelines for their elimination. One result will be a better-defined design space, where the designer can make informed choices whether to invest effort into designing, e.g., clean clock domain boundaries, or into a more thorough SLT application after manufacturing.

### *B. Automated Generation of SLT Programs for Characterization of Parametric Device Properties (P5)*

Project P5 aims at generating SLT programs with desired characteristics and at exploring approaches to assess the quality of such test programs by means of special *coverage metrics*. The central challenge during generation is to obtain an SLT program that can fulfill the desired *extra-functional properties*, e.g., a certain power consumption profile. To this end, model-driven performance stress test generation techniques from high-level software architecture models are used. Such techniques originate from the software engineering domain; they have previously been applied to enterprise software [18].

Another concept from software engineering will be used for quality assessment of SLT programs: coverage metrics used for black-box integration testing in, e.g., automotive domain that bears similarities to the SLT scenario [19]. An interesting question is the utilization of self-awareness present in many modern SoCs into SLT. For instance, the test equipment could monitor the built-in sensors during test application and dynamically schedule more or less stress-inducing SLT programs depending on the measured temperature.

### *C. Design for Testing and Reliability in the Presence of Transistor Self-Heating for Advanced Technologies (P9)*

Existing state-of-the-art FinFET technology has enabled the semiconductor industry to continue transistor scaling below 7 nm. However, at such extreme feature sizes, FinFET technology reaches its limit and replacing it with another technology becomes inevitable. Among many innovations, nanosheet transistors have been already adopted by semiconductor vendors for the upcoming generations as is evidenced by the 3 nm node offered by Samsung [20].

The very confined 3-D structure that nanosheet provides enables an excellent control but it imposes a serious challenge when it comes to reliability. The excessive heat generated inside the transistor's channel faces a profound difficulty to escape outside and be dissipated because the gate fully surrounds the channel [21]. This, in turn, accelerates the underlying defect generation mechanism and largely reduces not only the circuit's reliability but it also shorten its entire lifetime. The key research questions, which this project aims at answering: (1) How we can unveil during testing whether the underlying transistors in the chip suffer from internal self-heating or not? (2) How can information from IC tests (e.g., wafer and parametric test) be employed by the fab to not only accurately predict IC yield but to also improve it?

## V. ASSOCIATE PROJECTS TO THE GRADUATE SCHOOL

The Graduate School is supported by basic research projects with different funding. These projects are associated with the Graduate School, cooperate with other GS-IMTR projects, and cover lifecycle test problems. Modern circuits show high variations in their functional and extra-functional parameters which complicate the distinction between defect and defect-free circuits over a lifetime.

The first associated project (PA1 in Fig. 1) focuses on the test challenges of innovative, highly scaled technologies during the offline stage of the device lifetime, which include pre- and post-silicon validation (PSV) and manufacturing test. In this project, cell libraries are characterized under different operating conditions for defect and defect-free cases and are further reused for evaluating the PSV-prototypes and the manufactured devices. Robust test techniques which can detect infant mortalities without affecting the yield are developed by employing advanced machine learning methods [22, 23].

Moreover, the failure rate does not remain constant and there is an increasing failure rate throughout the useful life with respect to modern and latest technologies. The second associated project (PA2 in Fig. 1) exploits the behavior changes, such as measured delays under different operating conditions, over the past lifetime in order to create a lifetime model that detects abnormal behavior. This project uses this information to evaluate the current health state of the device. The information about the current behavior is collected using an extensive number of non-functional instruments like sensors, aging monitors, and built-in self-test registers mostly already integrated into a device.

Reconfigurable scan networks (RSNs) [24] offer an efficient way to access these instruments as well the device's registers throughout the lifetime, starting from PSV and also during the test insertions shown in the upper part of Fig. 1. At the same time, improper integration of RSNs can affect the system-level dependability. The third associated project (PA3 in Fig. 1), establishes a methodology to integrate dependable RSNs for a given device considering the following dependability aspects:

- *Accessibility:* A single fault in an RSN can prevent extracting complete data from the device during PSV, or lead to inaccessibility of a runtime-critical instrument and consequently lead to a system failure. Therefore, it has to be ensured that an RSN provides robust access to the underlying device [25].
- *Testability:* To ensure reliable access and to prevent silent data corruption via RSNs, the RSN itself has to remain testable, as shown in [26].
- *Security Compliance:* The accessibility via RSNs may violate the security requirements placed by the designer, e.g., the data confidentiality of certain instruments and the allowed accessibility of specific users. The security compliance of an RSN with the device is analyzed, possible violations are identified [27], and an RSN is correspondingly modified in a cost-efficient way [28, 29].

## VI. Conclusion

The Graduate School Intelligent Methods for Test and Reliability at the University of Stuttgart provides a very unique research experience in which several institutes are working along with a tight collaboration with one of the world leaders in chip testing: Advantest. It will play a major role in advancing the different research areas in design for testing and design for reliability. It will open new doors for bridging the gap between artificial intelligence and chip manufacturing, which might profoundly impact the future of technology.

## Acknowledgement

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